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Air Stable Cross-Linked Cytop Ultrathin Gate Dielectric for High Yield Low-Voltage Top-Gate Organic Field-Effect Transistors

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We demonstrate the use of a cross-linking chemistry for an amorphous fluoropolymer gate dielectric, poly(perfluorobutenylvinylether) commercially known as Cytop. Spin-coated films of Cytop exhibit good gate insulating properties as well as provide excellent OFET operational stability. However, these devices operate at large voltages because the dielectric layer thickness is typically ∼450−600 nm. When the thickness of a Cytop dielectric layer is decreased below 200 nm, the device yields are dramatically reduced due to pinhole formation. Our new cross-linked Cytop (C-Cytop) formulation deposited by spin-coating enables uniform thin films on top of various organic semiconductors that exhibits low gate leakage current densities (< 10 nA mm^{-2}) and high dielectric breakdown strengths (> 2 MV cm^{-1}). Our approach results in C-Cytop dielectric films as thin as 50 nm, thus allowing the fabrication of reliable p- and n-channel top-gate OFETs operating at very low-voltages (< 5 V). The most remarkable properties of this new C-Cytop gate dielectric are the excellent device yields (∼100%) for thicknesses < 100 nm and the dramatically reduced sensitivity to the underlying semiconductor film morphology. This new approach represents a significant advance compared to cross-linked PMMA films (C-PMMA) and other nonfluorinated polymer dielectrics on identical test structures. Furthermore, C-Cytop-based OFETs exhibit reduced bias stress and better air stability with respect to C-PMMA because of the inert perfluorinated chemical structure of this polymer. Finally, direct spectroscopic evidence of the cross-linking process was obtained by Fourier transform infrared (FTIR) spectroscopy, demonstrating complete reaction in air and at room temperature.

Introduction

Solution-processed organic field-effect transistors (OFETs) are being investigated for low-cost production on flexible substrates.[1−7] Field-effect mobilities as high as in amorphous silicon and other low-temperature processed metal oxides such as ZnO have been achieved with organic semiconductors, thus making OFET-based electronics attractive for diverse new applications.[8−13] Their successful integration into active matrix backplanes for various display technologies, including organic light-emitting diodes, liquid-crystal, and electrophoretic displays has been demonstrated.[14−17] Several studies have addressed the development of high performance and

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environmentally stable organic semiconductors for OFETs via molecular design/engineering to achieve enhanced intermolecular $\pi-\pi$ stacking and optimized film morphology.[1,13,18] Equally important, however, is the availability of high-performance gate dielectrics. A technologically relevant gate dielectric material should not only exhibit low charge trap density and negligible leakage currents (a prerequisite to enhance mobility and device performance for a given organic semiconductor), but must be solution-processable, compatible with both p- and n-channel semiconductors, and enable high device yields over large areas. SiO_2 has been the preferred gate insulator for OFET fabrication due to its excellent insulating properties and availability. Furthermore, it was shown that organic semiconductor performance could be significantly improved by modifying the SiO_2 surface with hydrophobic self-assembled monolayers (SAMs) such as hexamethyldisilazane (HMDS) or octyltrichlorosilane (OTS).[19−21] However, SiO_2 is not a practical solution for OFETs because of its incompatibility with low-temperature processing on inexpensive substrates.[10] Furthermore, because the field-effect mobility generally depends on the dielectric constant κ of gate dielectric as well as on chemical and morphological semiconductor/dielectric interface properties affecting charge trapping, the selection of proper gate dielectric materials to optimize transistor performance is of prime importance.[5,22,23]

The availability of high-performance, solution-processed polymer gate dielectrics is now considered a prerequisite to enable commercially relevant OFET-based devices.[24−27] However, polymer gate dielectric-based OFETs are typically limited by high operating voltages ($> \pm$ 20 V) as a result of the low capacitance of the thick gate dielectric films (usually $>$200 nm) needed to achieve sufficiently low pinhole and defect densities. Different approaches have been employed to lower OFET operating voltages including reducing polymer gate dielectric thickness[28,29] while preserving good insulating behavior, using self-assembled mono/multilayer dielectric films,[30,31] and employing high-κ gate materials.[32,33] Several groups have used cross-linkable polymer blends to achieve thin film thicknesses $<$ 50 nm and high breakdown voltages. However, these formulations are normally employed to fabricate bottom-gate device architectures in which the gate dielectric film is prepared on ultrasmooth substrates such as a highly doped Si wafer.[29,34,35] It is challenging to use cross-linkable polymers to fabricate top-gate transistors because of (i) possible organic semiconductor decomposition by the cross-linking agent/chemistry, (ii) the need to select an orthogonal solvent to prevent the dissolution and swelling of the organic semiconductor film, and (iii) the need to control leakage currents in the presence of different semiconductor film morphologies and surface roughness. Recently, Noh et al.[36] adapted an approach to ultrathin polymer gate dielectrics developed by Yoon et al.[29] to top-gate OFETs. This is based on blends comprising conventional insulating polymers and a cross-linking reagent based on bifunctional organosilanes.[37] In this system. the cross-linking chemistry takes places at room temperature in air by spontaneous formation of a 3D network, thus avoiding subjecting the underlying semiconductor to high temperatures. However, one major drawback of this method is that it is not always possible to find orthogonal solvents, particularly to some solution-processable small molecule organic semiconductors. Therefore, p-channel organic FETs based on TIPS-pentacene[38] and n-channel organic FETs based on PDIR-CN_2[39] are often confined to the use of fluorosolvents for top-gate dielectric processing as the only solvent exhibiting sufficient orthogonality. However, the device yields of this process is strongly dependent on the roughness of the underlying semiconducting layer.[36]

Experimental Section

Materials and Device Preparation. The fluoropolymer poly(perfluorobutenylvinylether) (Cytop, CTL-809M) and a perfluorocarbon-containing solvent (CT-Solv.180) were supplied by Asahi Glass and used as the gate dielectric. 1,6-bis(trichlorosilyl)hexane (C_6−Si) was purchased from Acros Organics and

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used as the cross-linking reagent. The semiconducting materials poly(9,9-dioctylfuorene-co-bithiophene) (F8T2) from Sumitomo Chemicals and ActivInk N1400 from Polyera Corporation were chosen as organic semiconductors. All materials were used as received without any further purification. Corning 1737F glass was used as the substrate for all devices after thorough cleaning in an ultrasonic bath with deionized water, acetone, and isopropanol, for 10 min each. The gold source and drain electrodes were patterned by a conventional double-layer photolithography lift-off process. The semiconducting materials were dissolved in anhydrous xylene (7 mg mL^{-1}, F8T2) or dichlorobenzene (7 mg mL^{-1}, N1400) respectively. The spun film of F8T2 (2000 rpm, 60 s) was annealed at 80 °C for 10 min to remove the residual solvent. For the spun film of N1400 (1500 rpm, 8 s), we first annealed it at 120 °C for 1 min to remove the solvent and then at 110 °C for 4 h to achieve high molecular ordering. To prepare 50−70 nm thick C-Cytop films, Cytop was first mixed with CT-Solv.180 at 1:3 volume ratio and then blended with 1,6-bis(trichlorosilyl)hexane (5−7 μL per ml) and the suspension left on a hot plate at 100 °C overnight to completely dissolve the cross-linking reagent. All the above processes were carried out in a nitrogen glovebox. Afterward, the C-Cytop solution was spun at 2000 rpm for 60 s onto the organic semiconductor films and annealed at 100 °C on a hot plate for 10 min to remove the solvent and fully complete the cross-linking process in air. Top-gate transistors were completed by evaporating 20 nm thick aluminum as gate electrodes through a shadow mask. The metal−insulator−metal (MIM) diodes were prepared by first evaporating a 30 nm patterned gold electrode on glass substrates, spinning thin C-Cytop films on top and then evaporating a patterned 20 nm thick aluminum electrode . For comparison of device yields, reference F8T2 devices with 50 nm thick C-PMMA were prepared as described in reference.[36] Samples for FTIR measurement were fabricated by spin-coating (2000 rpm, 60 s) 3:1 volume ratio of Cytop: CT-Solv.180, C-Cytop and pure C_6−Si solutions on top of double-side polished silicon substrates, either in the glovebox or in air, which gave film thicknesses around 450−500 nm (Cytop and C-Cytop) and 100 nm (C_6−Si).

Film and Device Characterization. The electrical characteristics of the transistors were measured in a nitrogen glovebox on a Karl-Suss probe station with an HP 4155B semiconductor parameter analyzer and HP4192A impedance analyzer. The transistor parameters, such as charge carrier mobility, were calculated using the standard formalism of field-effect transistors in the linear and saturation regimes respectively. The surface morphology of the films was obtained with a Veeco Dimension 3100 atomic force microscope (Digital Instruments) operated in the tapping mode. The thicknesses of the polymer films were measured with a Sloan Dektak Surface Profiler and the wettability of each surface was characterized by measuring the static contact angles using a contact angle goniometer (KSV Instruments). FTIR spectra were collected using a Thermo Nicolet Nexus 870 Fourier Transform Infrared spectrometer. The spectral range of the setup was determined by the type of beam splitter and detector, normally in the range of 400−6000 cm^{-1}. The spectra shown in this paper were typically taken from the average of 100 scans.

Results and Discussion

This study began by optimizing the fabrication of thin-films of C-Cytop. Figure 1a shows the molecular structure of Cytop and the cross-linking reagent, 1,6-bis(trichlorosilyl)hexane (C_6−Si). C-Cytop precursor solutions are prepared by dissolving Cytop (CTL-809M, low molecular weight for spin-coating, 9% concentration, Asahi Glass) in its fluorinated solvent (CT-Solv.180, Asahi Glass), which is orthogonal to most organic semiconductors, and then blending them in a nitrogen glovebox with C_6−Si at a suitable ratio. C_6−Si is poorly soluble in this fluorinated solvent; it requires several hours of stirring at 100 °C to achieve complete dissolution. However, when prepared these solutions are stable for several weeks (vide infra). Thin films of C-Cytop, ranging from 50 to 250 nm, can be deposited by spin-coating of these solutions in ambient conditions (Table 1). The principal chemical reaction of C_6−Si is illustrated in Figure 1b. The reactant molecules cross-link upon moisture-promoted self-condensation, providing a physical network embedding the Cytop fluoropolymer chains.[29,36,37]

The dielectric strength of C-Cytop vs un-cross-linked Cytop films was tested by measuring the current density versus electrical field (J-E) characteristics (Figure 1c) of these films in metal−insulator−metal (MIM) capacitors. In a thickness range between 50 and 150 nm, C-Cytop films exhibit breakdown fields > 2 MV cm^{-1} and leakage currents < 100 nA mm^{-2}. The 250 nm thick C-Cytop and 450 nm un-cross-linked Cytop films exhibit even higher dielectric breakdown strength (> 5 MV cm^{-1}) and lower gate leakage currents. The leakage current density of C-Cytop at 2 MV cm^{-1} is comparable to that of a plasma-grown aluminum oxide insulator with a phosphonic acid-based self-assembled monolayer[40] and to C-PMMA,[36] but significantly lower than that of other cross-linked polymer dielectrics, such as cross-linked PVP and cross-linked PVA.[34] Surprisingly, although C-Cytop and C-PMMA films exhibit similar leakage currents, we will show that MIM diode and OFET device yields based on C-Cytop are greatly improved.

To demonstrate the general applicability of C-Cytop dielectrics, OFETs were fabricated using two semiconductors differing in majority carrier type (p- and n-channel), chemical architecture (polymer and small-molecule), and film morphology (amorphous and crystalline, respectively). Figure 2a,b shows the transfer and output plots of an amorphous polyfluorene (poly(9,9-dioctylfluorene-co-bithiophene, F8T2, p-channel semiconductor) top-gate FET with a 50 nm thick C-Cytop dielectric. The transfer characteristics exhibit a steep current increase in the subthreshold region with low gate leakage currents, and the output characteristics show good saturation behavior even for short (2 μm) channel length devices. These FETs exhibit saturation mobilities (μ_{sat}) of $\sim 5 \times 10^{-3}$ cm^2 $V^{-1}s^{-1}$, which is typical for F8T2,[36] a very small threshold voltage (V_{th}) of −1.1 V, and a current on−off ratio (I_{on}:I_{off}) of 1×10^4 to 1×10^5 over a small voltage range (< -10 V) because of the high dielectric film capacitance ($C_i \approx 45$ nF cm^{-2}). Furthermore, both the transfer and output plots exhibit negligible

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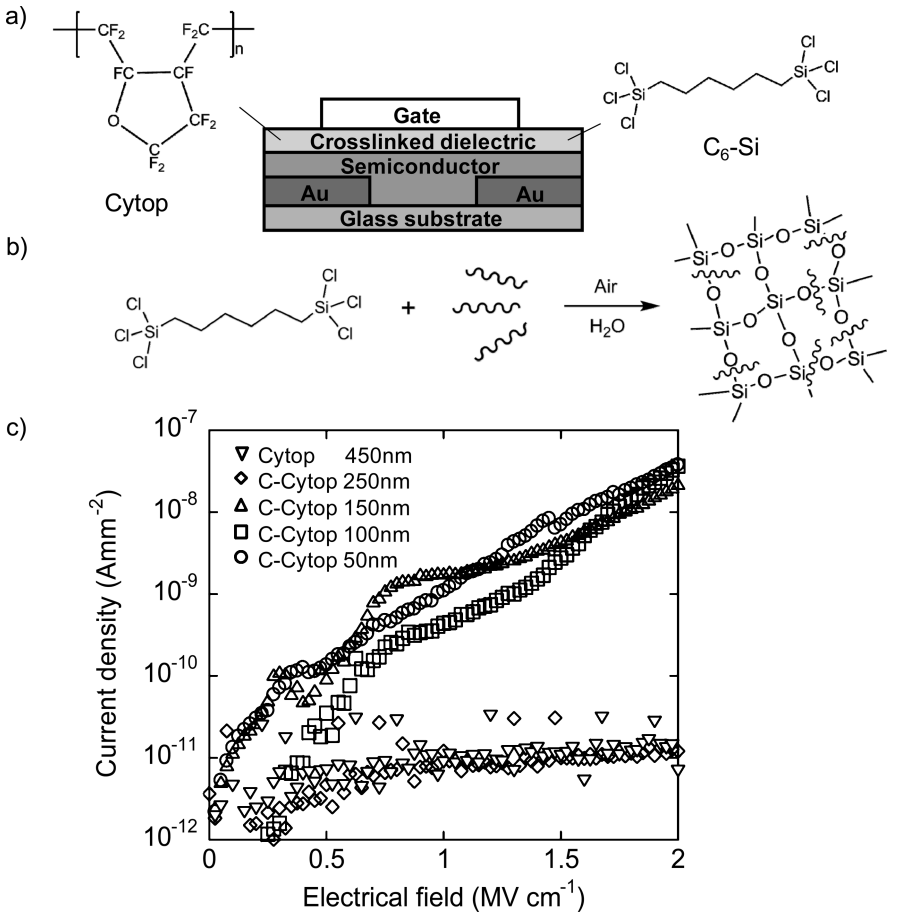

Figure 1. (a) Molecular structure of poly(perfluorobutenylvinylether) (Cytop) and 1,6-bis(trichlorosilyl)hexane (C_6−Si), used as gate dielectric and cross-linking reagent, respectively, and schematic diagram of the top-gate polymer transistor architecture used in this study. (b) Schematic of the cross-linking process of Cytop with C_6−Si when exposed to air. (c) Current density versus electric field (J−E) characteristics of gold MIM structures with thin films of Cytop (450 nm) and C-Cytop (from 50 to 250 nm).

Table 1. Summary of Gate Dielectric Properties of Cytop and C-Cytop

solution ratio (Cytop: solvent)	film thickness (nm)	rms roughness (nm)	capacitance (nF cm^{-2})
Cytop 3:1	450−500	0.42	5
C-Cytop 1:1	250−270	0.65	10
C-Cytop 1:2	130−150	0.63	28
C-Cytop 1:3	50−70	0.68	45

I−V hysteresis, indicating negligible charge traps are introduced by the cross-linking process. The operating gate voltage of −10 V used in these I−V measurements is equivalent to an electric field of ~2 MV cm^{-1} with 50 nm C-Cytop, and in these conditions gate leakage currents that are 1000× lower than the drain currents are observed. The excellent performance of C-Cytop films down to 50 nm is a combination of the good dielectric properties of the Cytop fluoropolymer and dielectric strength enhancement achieved by the C_6−Si cross-linked network.

One of the benefits of using Cytop solutions is that its fluorinated solvent is sufficiently orthogonal to most organic semiconducting materials, including very soluble small-molecule semiconductors. Because of this property, thin C-Cytop gate dielectric films could be used to fabricate top-gate n-channel OFETs based on a soluble small-molecule core-cyanated perylenediimide (ActivInk N1400, n-channel semiconductor). Figure 2c,d also shows the transfer and output plots of polycrystalline N1400 top-gate transistors with a 50 nm thick C-Cytop dielectric. These n-channel FETs operate at $V_g < 5$ V and the transfer plot demonstrates sharp electron current increase starting from $V_d = 1$ V and gate leakage currents < 100 nA. Electron mobilities as high as 0.01 cm^2 V^{-1} s^{-1} at $V_d = 5$ V for a channel length of 2 μm are extracted with a dielectric capacitance (C_i) of 45 nF cm^{-2}; V_{th} is as small as 0.5 V and the on−off ratio is as high as 1×10^5 to 1×10^6. For FETs with 20 μm channel lengths even higher electron mobilities of ~0.06 cm^2 V^{-1} s^{-1} are measured, indicating that the current in the short channel devices is limited by contact resistance.[6]

Previous studies have shown that the leakage current in a top-gate transistor configuration is very sensitive to the roughness of the underlying semiconductor film.[36] An atomic force microscopy (AFM) image of a 450 nm un-cross-linked Cytop film spun on a glass substrate is shown in Figure 3a. This data confirms that Cytop films are very smooth with a surface rms roughness (R_{rms}) of only 0.49 nm. The surface morphology of a 50 nm C-Cytop film on glass (Figure 3d) is slightly rougher with a R_{rms} of ~0.68 nm. Several raised topographic features

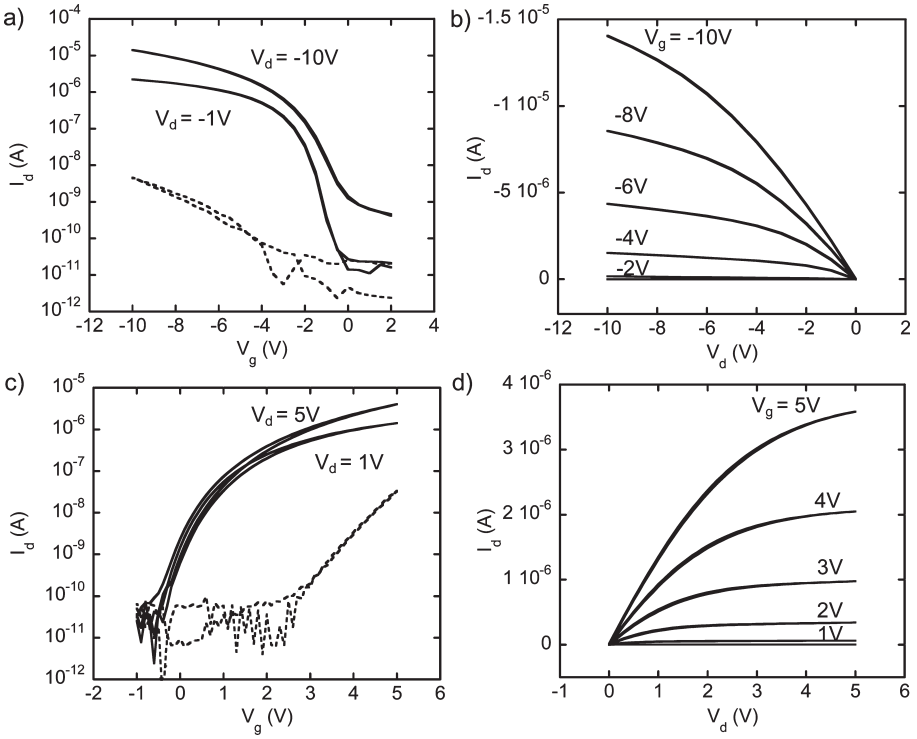

Figure 2. Electrical characteristics of F8T2 and N1400 top gate transistors (W/L = 10 mm/2 μm) with C-Cytop gate dielectrics (50 nm). (a, b) Transfer and output characteristics of a F8T2 transistor, (c, d) transfer and output characteristics of a N1400 transistor. The gate leakage currents (dashed line) were plotted at $V_d = -1$ V and $V_d = 1$ V, respectively.

can be identified in the C-Cytop film, probably arising from the cross-linked C_6−Si network. However, the remaining areas of the C-Cytop film are smooth and pinhole-free, which is considerably different than the morphology of most spin-coated polymer dielectrics of comparable thickness. The smooth film morphology and absence of pinholes is essential to minimize leakage current. The morphology of the semiconductor films used in this study has also been investigated. F8T2 polymer films (Figure 3b) exhibit a typical amorphous surface morphology with $R_{rms} = 0.83$ nm. In contrast, the polycrystalline N1400 small molecule films (Figure 3c) show a highly textured polycrystalline morphology and a greatly increased R_{rms} of 3.49 nm. Finally, the morphologies of C-Cytop films deposited on top of the semiconductors, which is the most relevant in OFET devices, were investigated. Going from the amorphous F8T2+C-Cytop to the polycrystalline N1400+C-Cytop bilayer films (Figures 3e and 3f, respectively) the R_{rms} increases from 1.55 nm to as high as 5.19 nm. However, we found that the increased N1400+C-Cytop film roughness does not compromize the leakage currents or failure rates of the corresponding top-gate transistors. The difference in transistor leakage currents between F8T2- and N1400-based devices is less than 10 nA and high transistor performance is achieved in both cases. This indicates that the OFET yields of thin C-Cytop-based devices are significantly less dependent on the surface morphology of the underlying semiconductor than previously observed for C-PMMA.[36] We believe that this might be a consequence of the low surface energy of the fluoropolymer, which provides conformal coverage of the underlying layer without generating pinholes or other thin film instabilities.[41] To support this point, we have also fabricated OFETs using a thin gate dielectric of polycyclohexylethylene (PCHE) cross-linked with the same protocol. PCHE is an hydrophobic low-κ dielectric material that exhibits a higher surface tension than Cytop (Cytop $\sim$ 19 mN/m and PCHE 30−40 mN/m). When used as the top-gate dielectric layer,[42] 100 nm thick cross-linked PCHE (C-PCHE) films do afford high-performance F8T2- and N1400-based OFETs (Figure 4). However, the device yields and stability are poor, supporting our argument that the polymer surface energy plays a key role when downscaling the dielectric thickness.

To further understand the details of the cross-linking reaction, we have investigated the difference in film composition of a pure C_6−Si and C-Cytop films before and after cross-linking using Fourier transform infrared (FTIR) spectroscopy. The typical FTIR spectra of un-cross-linked C_6−Si (fabricated in the glovebox) and cross-linked C_6−Si (fabricated in air) films are shown in Figure 5a. Without exposure to ambient moisture, which induces the cross-linking, there are almost no absorption peaks observed in the un-cross-linked C_6−Si spectrum between 500 and 5000 cm^{-1}. After the C_6−Si film is cross-linked in air, two peaks at 2860 and 2930 cm^{-1} appear in the FTIR spectrum, which are mainly related to the C−H

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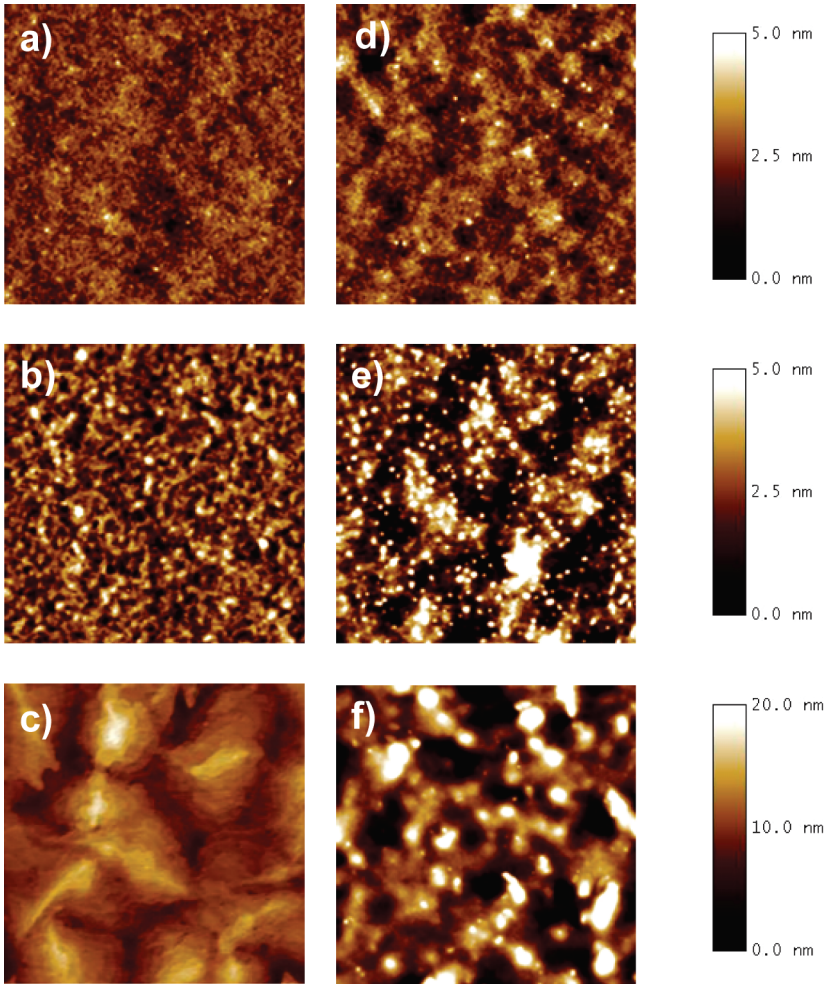

Figure 3. Atomic force microscopy images (2 μm × 2 μm) of surface morphology of (a) Cytop (~450 nm), (b) F8T2 (~80 nm), and (c) N1400 (~100 nm) on top of glass and surface morphology of C-Cytop (~ 50 nm) on top of (d) glass, (e) F8T2, and (f) N1400.

in-plane symmetrical (2860 cm^{-1}) and out-of-plane asymmetrical stretching (2930 cm^{-1}) vibrations.[43] This infrared absorption enhancement associated with the two C−H peaks reasonably arises from the $-CH_2-$ units next to the Si atoms. The reason for this C−H vibration enhancement is not completely clear yet, but we suggest that it may be due to the dipole moment changes going from Si−Cl before cross-linking to SiOH or Si−O−Si after cross-linking. In addition, cross-linked C_6−Si films exhibit a new broadband at 3400 cm^{-1} that is assigned to the silanol O−H stretching mode.[44] These results confirm the chemical reaction described by Yoon et al,[29] where the C_6−Si molecules cross-link in air to form a Si−O−Si network that physically embeds the dielectric polymer and residual Si−OH from uncondensed silane units. The FTIR spectra of pure Cytop and C-Cytop in Figure 5b further support the proposed mechanism for the cross-linking process. The C−H stretching vibration peaks at 2860 cm^{-1} and 2930 cm^{-1} are only found in the C-Cytop film, whereas all the other parts of the spectra show similar features.

Finally, we investigated both the device yield and stability of F8T2-based OFETs using C-Cytop and C-PMMA as the gate dielectric. Transistors were fabricated with different areas of overlap between the continuous gate electrodes and the active device region ranging from 0.06 to 0.4 mm^2 with at least 40 devices for each active area. Figures 6a and 6b show the transfer characteristics (including the gate leakage currents) of 10 representative OFETs across several batches. The overlap area (defined as the area of gate electrode overlapping with source-drain electrodes and the channel region) for these devices is 0.06 mm^2. The transistors with C-Cytop (Figure 6a) are obtained in ~100% yields, while several of the C-PMMA transistors (Figure 6b) exhibit unacceptably large gate leakage currents. When testing devices with even larger overlap area (0.4 mm^2), the thin C-Cytop film continues to function correctly, whereas the device yields of C-PMMA-based FETs is unacceptably low (Figures 6c and 6d).

Several studies have emphasized the low bias stress and stability of top-gate FETs based on Cytop.[45−47] We have also investigated the current and threshold voltage

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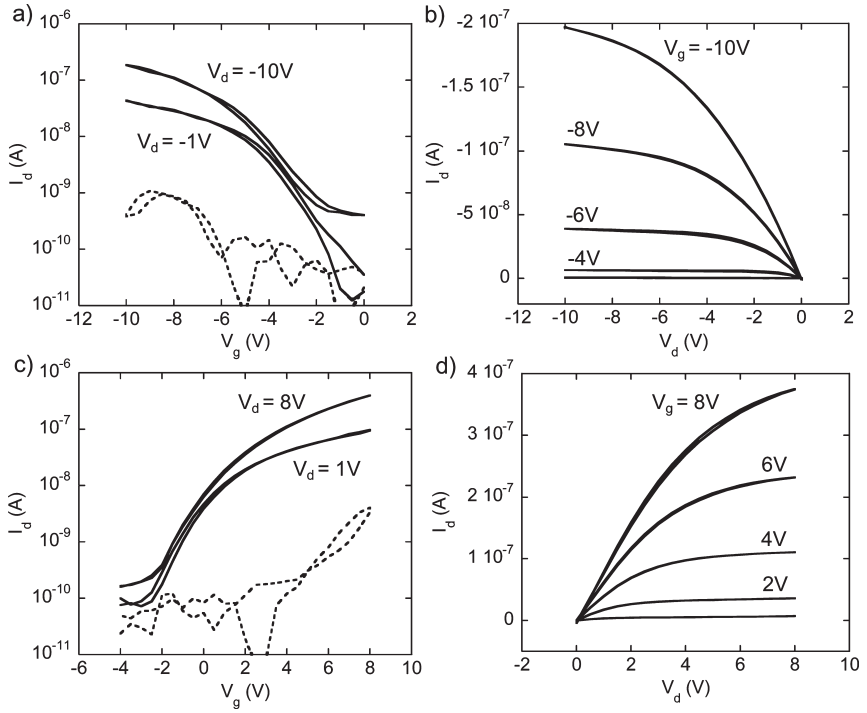

Figure 4. Transfer and output characteristics of F8T2 (a, b) and N1400 (c, d) top gate transistors (W/L = 1 mm/10 μm), using cross-linked PCHE (C-PCHE, PCHE blended with C_6−Si prepared in the same conditions as C-Cytop) as gate dielectric (100 nm).

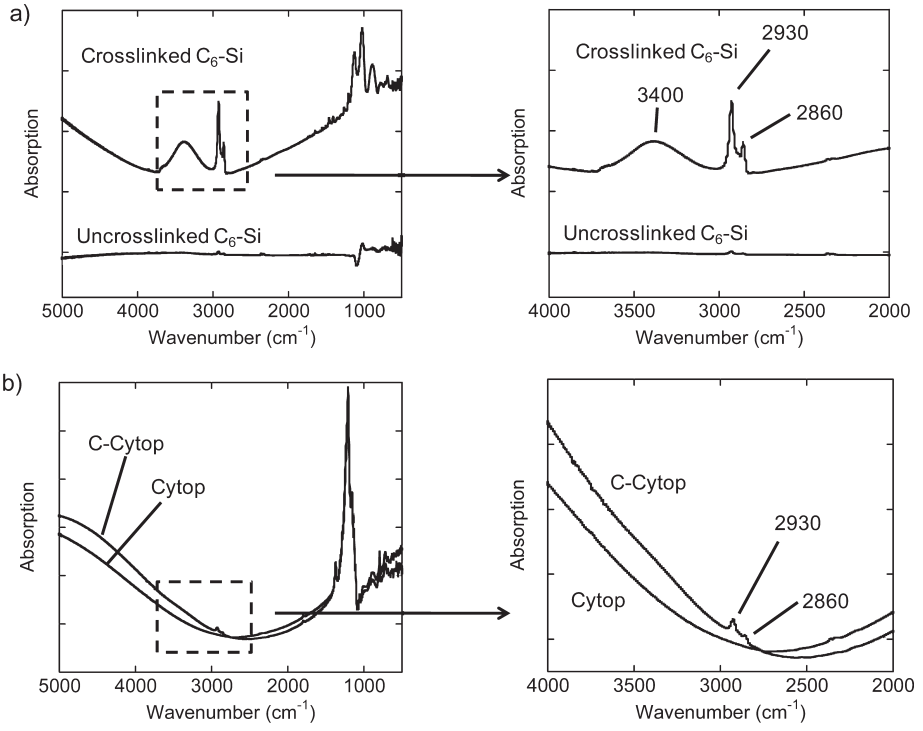

Figure 5. FTIR spectra of C_6−Si and C-Cytop films spun on silicon substrates. (a) Un-cross-linked C_6−Si prepared in a glovebox and cross-linked C_6−Si prepared in air; (b) pure Cytop prepared in a glovebox and C-Cytop prepared in air. The peaks at 2930 and 2860 cm^{-1} are related to the C−H stretching vibrations from the backbone of C_6−Si.

stability of F8T2 FETs with C-Cytop and C-PMMA devices. For this study, continuous biases (V_g = −10 V and V_d = −1 V) were applied to these FETs over a 3 h period in the dark and in the glovebox. Figure 7a shows that the drain current of C-PMMA transistors decreases much faster ($I/I_0 \sim 0.4$) during the bias stress measurements than for the devices with C-Cytop ($I/I_0 \approx 0.7$). The comparative stability of C-Cytop vs C-PMMA F8T2 FETs was also tested after exposing the devices to the air for 12 h. Figure 7b shows that transistors with C-Cytop degrade far less rapidly ($I/I_0 \approx 0.8$) then those with C-PMMA ($I/I_0 \sim 0.5$). The improved stability of C-Cytop devices is attributed to the perfluorinated polymer structure, which provides better encapsulation against moisture permeation (moisture permeation coefficient: Cytop = 1.1×10^{-12} and PMMA = 3.2×10^{-9} cm^3 cm/cm^2 s Pa,

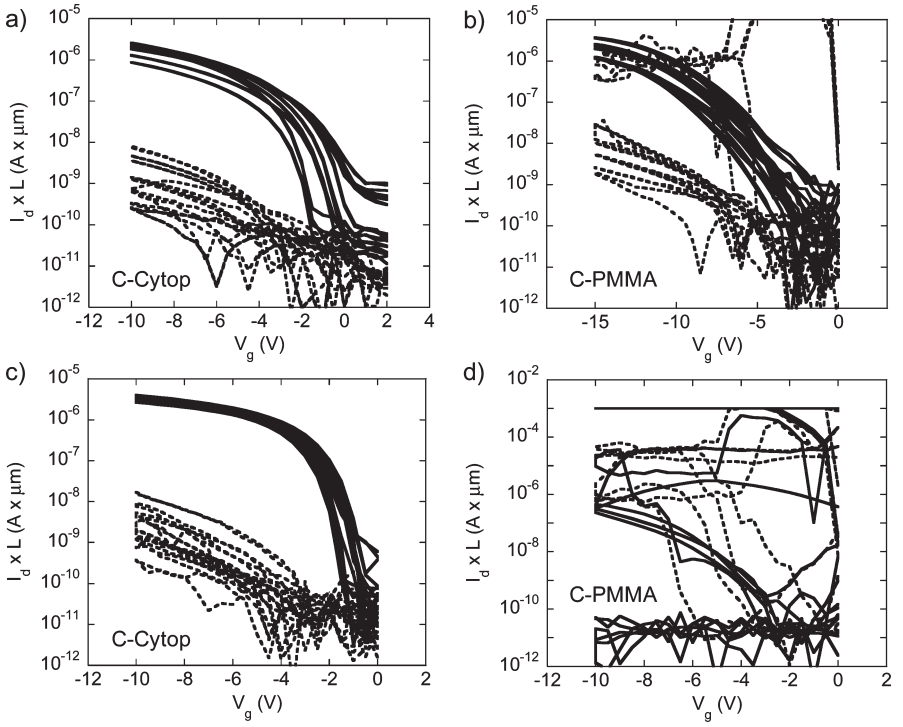

Figure 6. Comparison of F8T2 FET yield for devices with C-Cytop and C-PMMA as the gate dielectrics. (a, c) Top gate transistors with a 50 nm thick C-Cytop dielectric; (b, d) Top gate transistors with 50 nm C-PMMA. Devices a and b have a small overlap area of 0.06 mm^2 (W/L = 1 mm/10 μm, V_d = −10 V), whereas devices c and d have a large overlap area of 0.4 mm^2 (W/L = 10 mm/10 μm, V_d = −1 V), and each plot contains 10 transfer characteristics of the devices measured in the glovebox.

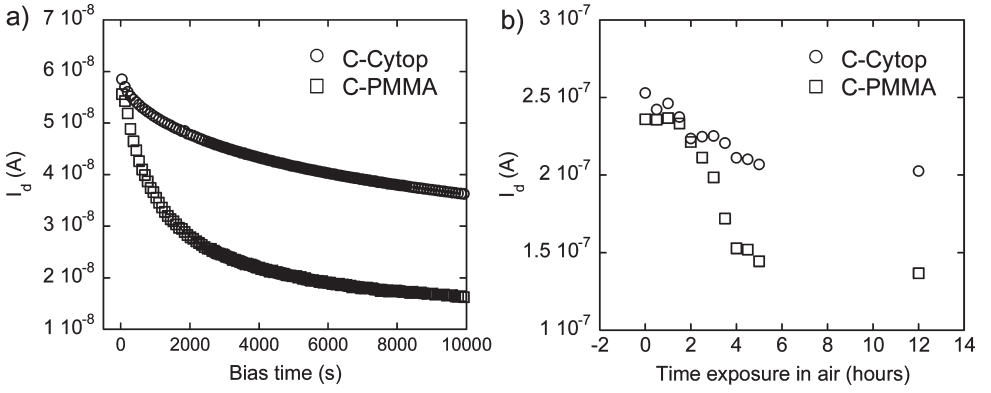

Figure 7. Comparison of F8T2 FET stability for devices with C-Cytop and C-PMMA as gate dielectrics (W/L = 1 mm/10 μm). (a) Corresponding bias stress measurements for both devices in the glovebox (V_d = −1 V and V_g = −10 V). (b) Corresponding stability data for both devices in ambient (V_d = −10 V and V_g = −10 V).

Asahi Glass) and reduced energetic broadening of the semiconductor density of states at the dielectric interface.[48]

Conclusions

In conclusion, we have developed an approach to cross-link a fluoropolymer (C-Cytop) enabling the fabrication of top-gate transistors with ultrathin (< 100 nm thick) gate dielectric films in high yields (~ 100%). The devices based on both p- and n-channel semiconductors operate below |10 V| and exhibit field-effect mobilities and current on−off ratios comparable to the devices with thicker dielectric films. The orthogonality of the C-Cytop fluorinated solvent to conventional organic semiconductors allows fabrication of devices based on both polymeric and soluble small-molecule semiconductors. The main advantages of C-Cytop films are the reduced sensitivity of the dielectric strength on the underling semiconductor film morphology and the low charge trapping. Whether the device yield is high enough to be applicable on an industrial scale remains to be investigated, but our experiments performed on a laboratory scale certainly indicate that cross-linked fluoropolymers are an attractive candidate for ultrathin, solution-processable gate dielectrics for OFETs applications.

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